In-Sem Examination

Sub: VLSI Design & Technology

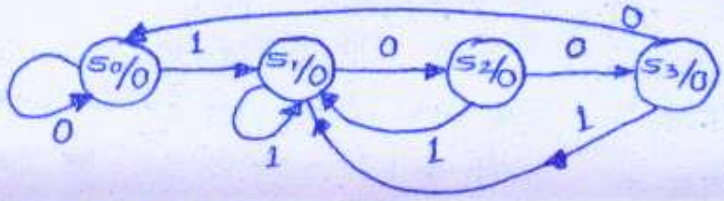
Class: BE E&Tlc (2012 Course)

Paper solution / Marking scheme

Q1. (a) Structural, behavioural & data flow.

(b) VHDL code : 3 Marks ; Test bench : 2 Marks

Q2. (a)



Students may assume overlap / non overlap type. Hence FSM diagram may vary, accordingly.

(b) Need : Optimized way & iteration.

Q3. (b) Criterion : Way of logic implementation, architectural blocks, interconnects, technology etc.

Q4. (a) Through product terms & LUTs.

(b) PAR : 3 Marks ; Timing : 2 Marks

Q5. (a) At least 5 issues.

(b) Need : Power reduction - 2 Marks

Method - 3 "

Q6. (a) Jitter : false trigger may take place.

(b) Any 2 methods are expected.

BE/InSem.-38

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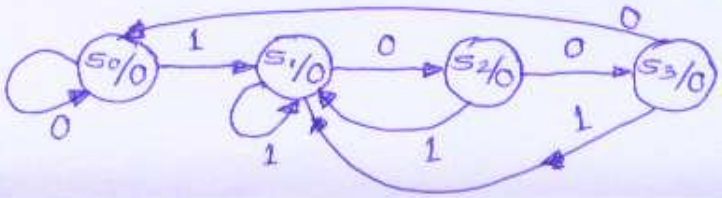

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